ENG17

UNIVERSITY OF BOLTON

SCHOOL OF ENGINEERING

M.Sc. ELECTRICAL & ELECTRONICS ENGINEERING

SEMESTER 2 EXAMINATION- 2022/2023

PERVASIVE EMBEDDED SYSTEM DESIGN

MODULE NO: EEE7007

Date: Thursday 11th May 2023 **Time: 10:00am – 12:30pm**

INSTRUCTIONS TO CANDIDATES:

There are SIX questions.

You should answer ANY FOUR questions.

All questions carry equal marks.

Marks for parts of questions are shown in brackets.

Graphical calculators are not allowed.

CANDIDATES REQUIRE: **Formula Sheet, Scientific calculator.**

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Question 1: Consider a system that acquires an analogue signal with a range of 0-5V and converts it into a digital signal using a 10-bit analog-to-digital converter (ADC) with a reference voltage of 5V. The system then sends the digital signal over a communication channel with a BW of 512 KHz with a maximum data rate of 10 Mbps.

a) What is the minimum time required to convert the analogue signal into a digital signal?

[8 marks]

b) What is the maximum frequency of the digital signal that can be transmitted over the communication channel?

[2 marks]

c) If the communication channel has a signal-to-noise ratio (SNR) of 40 dB, what is the maximum number of bits per sample that can be transmitted reliably?

[10 marks]

d) If the system needs to transmit the data with a higher data rate of 50 Mbps, what modifications would you suggest to the system?

[5 marks]

[Total = 25 marks]

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Question 2: You are aiming to join an embedded system design corporation in the UK. During the pre - interview stage you receive some compulsory questions to move to the next stage of the interview. The company mostly uses ARM based microcontrollers, and they want you to answer the questions below in detail. You are required to answer all questions**.**

(a) Describe the ARM Cortex-M architecture and explain how it differs from the traditional von Neumann architecture. Discuss the features of the ARM Cortex-M architecture that make it well-suited for use in embedded systems.

[10 marks]

(b) Discuss the differences between signed and unsigned number representation in binary number systems and explain how each type of representation can be implemented in an embedded system. Provide an example of a situation where signed and unsigned number representation can impact the design of an embedded system.

[12 marks]

(c) Convert the octal number 343 into a binary number by using the 3-binary digits method. Show your steps clearly.

[3 marks]

[Total = 25 marks]

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Question 3: A 3-bit ADC system voltage ranges between 0 to 16 V, answer the following questions. Show your calculation clearly in each question. Indicate the unit clearly, if appropriate.

a) If the measured voltage is 4.2V, what will the ADC value be? Use the formula below.

$$\frac{\text{Total number of quantisation levels}}{\text{Full Voltage Range}} = \frac{\text{ADC Reading}}{(\text{Analogue Voltage Measured} - \text{Min System Voltage})}$$

[5 marks]

b) What is the step size of the ADC system?

[5 marks]

c) If the ADC reading is 6, what will the range of the measured voltage be?

[5 marks]

d) Draw the graphical representation of quantization levels.

Indicate clearly the voltage on the Y-axis, the voltage range, the digital level and the numeric level.

[10 marks]

[Total = 25 marks]

Question 4: Please answer all parts of the question below:

a) Discuss the interrupt handling mechanisms used in the ARM Cortex-M architecture. Explain how interrupts are prioritized, how they are handled, and how they are serviced by the CPU. Give an example of how interrupts could be used in an embedded system.

[15 marks]

b) Explain the role of the memory management unit (MMU) in the ARM Cortex-M architecture. Discuss the benefits of using an MMU in embedded systems and how it can be used to protect against security threats.

[10 marks]

[Total = 25 marks]

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Question 5: Please answer all parts of the question below:

a) Suppose you are working on an embedded system that uses an ADC to convert an analogue signal to a digital value. The ADC has a resolution of 12 bits and a reference voltage of 3.3 volts. If the input analogue signal ranges from 0 to 2 volts, what is the step size of the ADC?

[10 marks]

b) Explain the difference between analogue and digital signals in embedded systems. What are the advantages and disadvantages of using each type of signal in an embedded system? Provide an example of a situation where one type of signal would be preferable over the other.

[10 marks]

c) Suppose you are working on an embedded system that requires a digital signal to be sent to a motor control circuit. The motor control circuit requires a minimum voltage of 3.5 volts to activate. If the microcontroller in the embedded system uses 3.3 volts as its logic high voltage, what is the minimum number of bits required to represent the digital signal to the motor control circuit?

[5 marks]

[Total = 25 marks]

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Question 6: Please answer all parts of the question below:

a) Suppose you are working on an embedded system that uses a digital-to-analogue converter (DAC) to convert a digital signal to an analogue voltage. The DAC has a resolution of 10 bits and an output voltage range of 0 to 5 volts. If the digital signal is represented by the value 512, what is the corresponding output voltage?

[6 marks]

b) Explain the concept of signal conditioning in embedded systems. What are the different types of signal conditioning techniques used in embedded systems, and how do they help improve the quality and reliability of signals? Provide an example of a situation where signal conditioning would be necessary.

[12 marks]

c) Suppose you are working on an embedded system that requires a digital signal to be sent to a LED driver circuit. The LED driver circuit requires a minimum current of 10 mA to activate. If the microcontroller in the embedded system can supply a maximum current of 5 mA per output pin, what is the minimum number of output pins required to drive the LED driver circuit? Assume that each output pin can be set to either high or low to control the LED driver circuit.

[7 marks]

[Total = 25 marks]

END OF QUESTIONS

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Formula Sheet:

- *I_avg = (I_active * T_active + I_sleep * T_sleep) / (T_active + T_sleep)*
- *I_avg * operation time*
- *Conversion time = 1 / Sample rate*
- *SNR_linear = 10(SNR_dB/10)*
- *T = 1/F*
- $F_{sample} \geq 2 * F_{max}$.
- $F_{Max} = BW/2$
- C = B * log2(1 + SNR).
- $B_{max} = C / F_{sample}$, where C is the channel capacity.
- $\frac{\text{Total number of quantisation levels}}{\text{Full Voltage Range}} = \frac{\text{ADC Reading}}{(\text{Analogue Voltage Measured} - \text{Min System Voltage})}$
- *Voltage range per possible value = Reference voltage / Total number of possible values*
- *n = log2((Vmax / Vhigh) + 1)*
- Total current = Number of output pins x Maximum current per output pin

END OF PAPER